Analysis of MLSA for Low Power CAM Design

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ABSTRACT

In single clock cycle a high speed search function is obtained in Content addressable memory (CAM). It is power-hungry because of its parallel match line sensing. Thus, we analyze several Match Line sensing designs to predict which covers less area, power and delay. In Gated power ML sensing power, area and delay can be reduced as compared to other method. The power supply to the comparison elements will be automatically turned off by using the concept of feedback loop.

KEY WORDS: Content Addressable Memory (CAM), Voltage Controlled current Source (VCCS), Current Saving Control (CSC).

1. INTRODUCTION

In Content Addressable Memory the search can be done in parallel manner by comparing the search data with the stored data. CAM is having a search line (SL) and the match line (ML) for getting the data to be searched as well as to display the matches and mismatches. The data to be searched is stored in the search word register and it consumes more power due to its parallel search. The fig.1, represents the conventional CAM with the search data register, encoder and Match Line Sense Amplifier (MLSA). The search word register stores the n-bit data and starts the comparison by broadcasting the word in the search line to match with the stored word. With the help of encoder the matched or mismatched conditions can be identified. Initially the ML should be pre-charged to ground and both SL and ~SL to VDD. During the Evaluation stage broadcast starts in the SL. If both the data match then no changes occurs in the ML. Suppose mismatch happens then the transistor P3 and P4 gets ON and ML is directly connected to VDD. MLSA sense the voltage change in the ML and amplify it to a full CMOS voltage output. If there is any mismatches happen then the ML value won't be change since there is no path from VDD to ML.

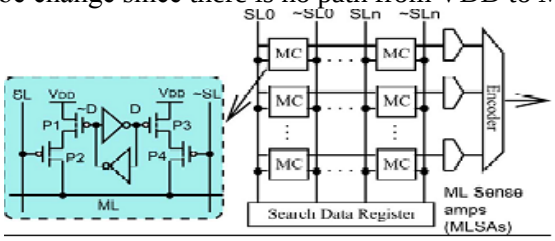

Figure.1. Conventional CAM

In order to reduce the power consumption in CAM we have to reduce the switching capacitance in the ML by using a NAND ML architecture. The architecture consists of several pass transistors in series, if data match then the signal from one end propagate to the other end but in case of mismatching the signal propagation has been stopped so power consumption can be avoided. As per in NAND architecture unacceptable search delay can be found, in order to avoid this and to achieve a high speed a NOR based architecture has to be used. A NOR based architecture is having comparison circuit that compares the data and justify that the data matches or not, if matches then the isolation of ML from Ground results in High impedance state of ML and mismatch sends the ML to Low impedance. This impedance changes can be observed properly by the sensing scheme thereby the reduction of speed with high power consumption. Various sensing scheme can be used to obtain the speed and power optimization.

Match line sensing:

Mismatch dependent power allocation: The architecture of mismatch dependent power allocation is shown in fig.2. Here the identical current source is used to differentiate between match and the mismatch. The ML with no mismatches ML_0 having high impedance will develop a voltage higher than the ML with one mismatch ML_1. The sensing circuit will differentiate that the ML_0 with high voltage and ML_n with voltage nearer to GND. The current saving block is added to each ML to reduce the charging current by sensing the voltage on that line. First the ML is reset to GND and precharge all sense nodes to VDD.

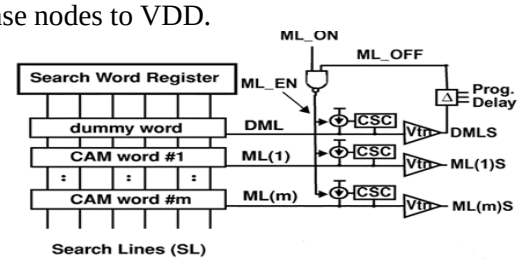

Figure.2. General architecture for ML power allocation

At the same time search data is delivering through SL to compare. The current source on each ML is enabled through $ML_{\_ON}$. The voltage V_{ML} on each line is varied in accordance with the number of mismatches, the ML voltage on ML_0 increased as a ramp crossing the sense threshold since it has no path to ground. The voltage on ML_n getting decreased to GND, the current source is disabled by giving the shut-off signal. This signal is generated when the data stored in the dummy word complete its comparison; it acts as a reference because the data stored in the dummy is same as search data. After this the voltage which crossed the sense threshold voltage marked as match and the signal near to sense threshold are also marked as no matches.

Further decrease of power is achieved by introducing a small energy on each ML to identify the state of ML. A dynamic current source having CSC and voltage-controlled current source (VCCS) fig.3, supplies the current to each ML, according to the mismatch the voltage will be generated and indicates the state of ML.

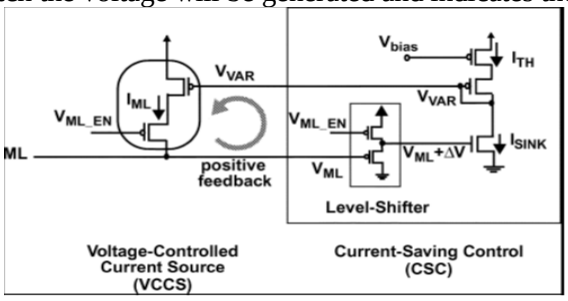

Figure.3. Dynamic current source

In circuit level implementation of dynamic current source, VCCS has two pMOS in which one acts as an enable switch and the other acts as variable I_{ML} control by using V_{VAR} node voltage V_{VAR} is produced by the CSC block by the comparison between the I_{SINK} and I_{TH}. I_{SINK} is produced in proportional to V_{ML} and I_{TH} is set as constant current by V_{bias}. A V_{ML} is converted into a constant V_{VAR}, if V_{ML} increases I_{SINK} also increases thereby reducing V_{VAR} and I_{ML} increases. Because of increase in I_{ML}, V_{ML} get further increase, creating a positive feedback loop. A level shifting circuit is introduced to eliminate the dead band from GND to V_{tn}.

Match sensing using Match-line Stability: In this method difference between match and mismatch is found by the resistance R_{CELL}/n which shunts the capacitance in case of n mismatch as shown in fig.4. Now the properties of ML model are observed in s-domain. From the fig.5, we observe that the ML should be a system with a current into the ML, $I_{ML}(s)$ as a input and the voltage $V_{ML}(s)$ as a output. The transfer function is given by

$$Z(s) = \frac{V_{ML}(s)}{I_{ML}(s)}$$

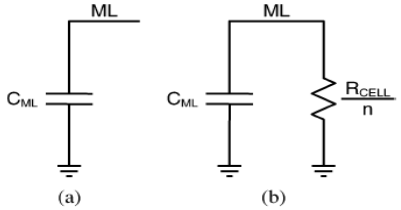

Figure.4. simplified ML model. a)Matched ML b)ML with n bits

Here the pole location depends upon the n mismatch. If there is no mismatch then the impedance depends only on the C_{ML} but mismatch occurs then impedance depends on both R_{CELL} and C_{ML}. The impedance of match and mismatch is given by

$$Z_{\text{MATCH}}(s) = \frac{1}{s \cdot C_{\text{ML}}}.$$

For an ML with n-bit miss, $n \geq 1$, we have

$$Z_{\text{MISS}}(s) = \frac{R_{\text{CELL}}/n}{1 + s \cdot C_{\text{ML}} \cdot R_{\text{CELL}}/n}.$$

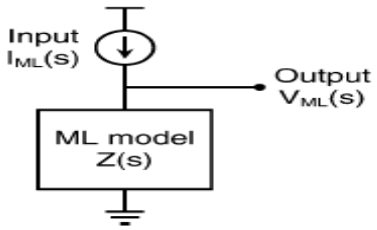

Figure.5. ML model in s-domain

From fig.6, ML with no mismatch has a pole at zero and ML with 1 mismatch has a pole on Left half plane (LHP).we know that the pole at zero is said to be marginally stable system and the pole in the LHP is said to be the

stable system. The output of stable system decays to zero and at the same time the output of a unstable system grows to VDD. In our concept the value of matched ML should be VDD and the value of the mismatched line depends on number of mismatches. But pole of matched line is at zero, we want to shift this pole to the RHP. For shifting we introduce a negative resistance $-R_{CELL}$. Now the pole is shifted as shown in fig.7.

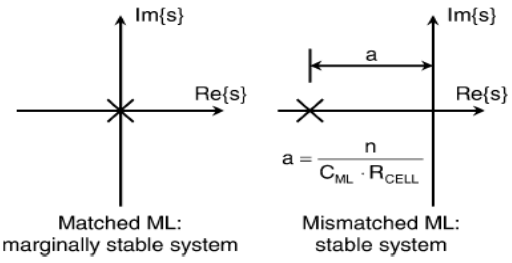

Figure.6. Pole location in ML model

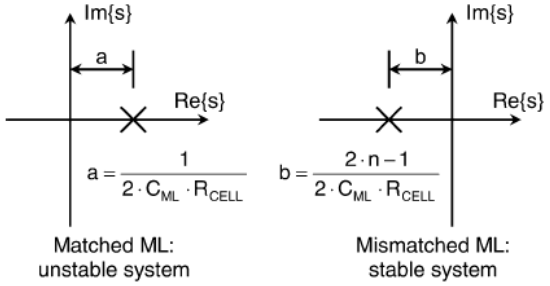

Figure.7. ML Pole location in stability-based sensing scheme

The ML having no mismatch is having high V_{ML} due to the capacitor C_{ML} getting charged through the negative resistance. If the mismatch occurs then the total resistance as

$$R_{TOTAL} = -2R_{CELL} \parallel R_{CELL} = 2R_{CELL}$$

The initial charge of the capacitor is dissipated by this positive resistance as shown in fig.8. The V_{ML} decays to ground. We can easily identify the match and the mismatch.

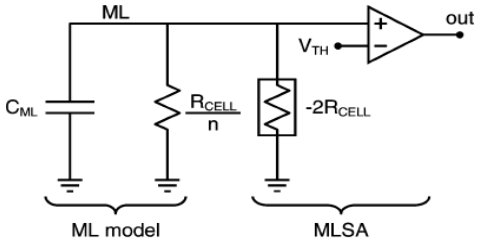

Figure.8. ML model in stability sensing.

The negative resistance circuit is shown in fig.9, which consists of level shifter, sensor to monitor threshold and negative resistance realization circuit. As per the fig EN signal is set to zero to turn off any current source at the same time RST signal is enabled high to pre-charge. The reset transistor N1 is used to reset the ML and a excitation pulse is used to supply initial energy to ML. If matches occurs voltage in ML increases otherwise voltage decreases to zero.

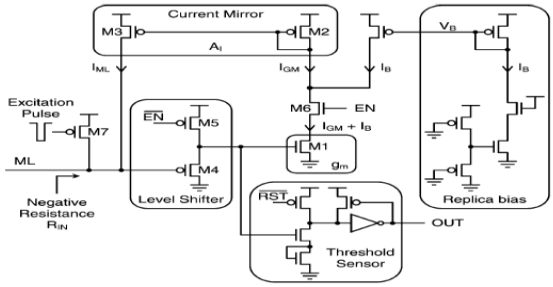

Figure.9. Transistor level circuit for negative resistance

Active feedback ML sensing: In this method all ML is charged by same current from current sources. As shown in fig.10 ML_0 charges very fast as compared to the ML_n and also the source to gate voltage of P6 transistor is very small for ML_0. The source to drain voltage of P6 transistor should be increased to maintain the I_{FB} through the P6 to be constant. The V_{CS} is getting smaller due to the presence of P6 source near to the VDD. This continuous until the voltage in the ML_0 reaches the threshold voltage so that the current sources are getting switched off.

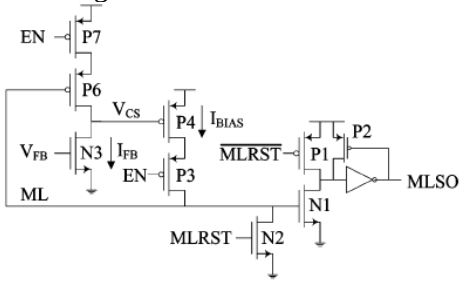

Figure.10. Active feedback MLSA

Gated power ML sensing: The gated power ML sensing as shown in fig.11, operates by setting enable as zero thereby making C1 and ML as VDD and GND. Then the enable signal is set high and at the same time the compare operation starts. Now the transistor P_x starts conducting VDD_x. If the mismatch occurs in any memory unit will enable a path from GND to VDD indicates the mismatch. The voltage in mismatch ML reaches the threshold voltage of transistor M8 and the node voltage C1 will be low and the NAND gate is made as high so that the power transistor is getting off.

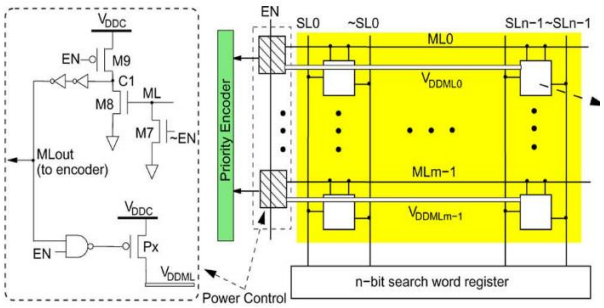

Figure.11. Gated Power architecture of CAM

2. RESULTS AND DISCUSSION

Table.1. Comparison of Related Works

Title	AREA (LE's)	Power (mW)	Delay
A High Speed Low Power CAM With a Parity Bit and Power-Gated ML Sensing	1034	58.84	0.74
A Mismatch Dependent Power Allocation Technique for Match-Line Sensing in Content-Addressable Memories	1324	74.24	1.07
Match Sensing Using Match-Line Stability in Content -Addressable Memories	1378	77.14	0.98
A Low-Power Ternary CAM With Positive-Feedback Match-Line Sense Amplifiers	1489	81.04	1.24

3. CONCLUSION

Thus the CAM Architecture has been reviewed by using several MLSA Devices, where the area, power, delay can be calculated. Out of those comparison, Parity Bit and Power-Gated ML Sensing offers better performance in various parameters like delay, area, and power .In future we planned to implement the segmentation of ML sensing in XORAM based CAM cell.

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